Serial No.: 10/672,103
Group Art Unit: 2826

AMENDMENTS TO CLAIMS

• Please amend pending claims 7-9, 13-16, and 18-20 as indicated below. A complete listing of all claims and their status in the application are as follows:

Claims 1-6 (canceled).

7. (currently amended) An integrated circuit comprising;

a substrate having a semiconductor device thereon;

a first stop layer over the substrate having a ~~portion open~~stepped opening to the semiconductor device;

a first dielectric layer over the first stop layer having an opening provided therein having sidewalls in the first dielectric layer;

a first conformal barrier liner in the opening, the first conformal barrier liner having only vertical portions of a constant thickness on the sidewalls of the opening in the first dielectric layer, the vertical portions of the first conformal barrier liner on the sidewalls acting as a barrier to diffusion of conductor core material to the first dielectric layer;

a treated area on the first conformal barrier liner and the first stop layer to increase adhesion properties thereof; and

a first conductor core in the opening over the vertical portions of the first conformal barrier liner and the first stop layer, the first conductor core connected to the semiconductor device.

8. (currently amended) The integrated circuit as claimed in claim 7 including:

a ~~via~~ second stop layer over the first dielectric layer and having an opening provided therein;

a ~~via~~ second dielectric layer over the ~~via~~ second stop layer and having an ~~via~~ opening provided therein having sidewalls;

a ~~second~~ third stop layer over the ~~via~~ second dielectric layer and having an opening provided therein;

~~a second dielectric layer over the via dielectric layer having a channel opening provided therein having sidewalls;~~

a second conformal barrier liner in the opening in the second dielectric layer, the second conformal barrier liner having only vertical portions of a second constant thickness on the sidewalls of the openings in the second dielectric layer and the ~~via~~ second dielectric layer;

a treated area on the second conformal barrier liner and the second stop layer for increasing adhesion properties thereof; and

~~a second~~the first conductor core in the opening over the vertical portions of the second conformal barrier liner~~, the first conductor core,~~ and the second stop layer, the second conductor core connected to the first conductor core through the opening in the via stop layer.

9. (currently amended) The integrated circuit as claimed in claim 8 wherein the first stop layer over the substrate has a thickness "t" and the ~~via~~ second stop layer has a thickness "T" of greater than about 2t.

10. (original) The integrated circuit as claimed in claim 7 wherein the first conformal barrier liner has a region selected from a group consisting of silicon-enriched, wetting layer covered, and a combination thereof.

11. (original) The integrated circuit as claimed in claim 7 wherein the first conformal barrier liner is a nonconductive barrier material selected from a group consisting of a nitride, a BLok, a carbide, an oxynitride, and a combination thereof.

12. (original) The integrated circuit as claimed in claim 7 wherein the first conductor core is a material selected from a group consisting of copper, aluminum, gold, silver, compounds thereof, and combinations thereof.

13. (currently amended) The integrated circuit as claimed in claim 7 wherein the first dielectric layer~~, the via dielectric layer, and the second dielectric layer are of~~ comprises a low dielectric constant materials.

14. (currently amended) An integrated circuit comprising;

a substrate having a semiconductor device thereon;

a device dielectric layer over the substrate;

a first channel stop layer over the substrate and the device dielectric layer having a ~~portion open~~stepped opening to the semiconductor device;

a first channel dielectric layer over the first channel stop layer having a first channel opening provided therein having sidewalls in the first channel dielectric layer;

a first conformal barrier liner in the opening, the first conformal barrier liner having only vertical portions on the sidewalls of the opening in the first channel dielectric layer, the vertical portions of the first conformal barrier liner on the sidewalls acting as a barrier to diffusion of conductor core material to the first channel dielectric layer;

a treated area on the first conformal barrier liner and the first channel stop layer to increase adhesion properties thereof; and

a first conductor core in the opening over the vertical portions of the first conformal barrier liner and the first channel stop layer, the first conductor core connected to the semiconductor device.

15. (currently amended) The integrated circuit as claimed in claim 14 including:

a via stop layer ~~over~~ under the first channel dielectric layer and having an opening provided therein;

a via dielectric layer ~~over~~ under the ~~via~~ first channel stop layer and having a via opening provided therein having sidewalls;

~~a second~~the first channel stop layer ~~over the via dielectric layer and~~ having a stepped opening provided therein, a first portion of the stepped opening of the same size as the opening in the first channel dielectric layer and a second portion of the stepped opening of the same size as the opening in the via stop layer;

~~a second channel dielectric layer over the via dielectric layer having a second channel opening provided therein having sidewalls;~~

a second conformal barrier liner in the via opening, the second conformal barrier liner having only vertical portions on the sidewalls of ~~the second channel opening and~~ the via opening ~~in the second channel dielectric layer and the via dielectric layer~~, the vertical portions of the second conformal barrier liner on the

sidewalls of the via opening acting as a barrier to diffusion of first conductor core material to ~~the second channel dielectric layer and~~ the via dielectric layer;

a treated area on the second conformal barrier liner and the ~~second~~ via stop layer to increase adhesion properties thereof; and

~~a second~~the first conductor core in the via opening over the vertical portions of the second conformal barrier liner~~, the first conductor core,~~ and the ~~second~~ first channel stop layer~~, layer, the second conductor core connected to the first conductor core through the opening in the via stop layer.~~

16. (currently amended) The integrated circuit as claimed in claim 15 wherein the via stop layer ~~over the substrate~~ has a thickness "t" and the ~~second~~ first channel stop layer has a thickness "T" of greater than about twice the thickness "t" distal from the stepped opening.

17. (original) The integrated circuit as claimed in claim 14 wherein the first and second conformal barrier liners have regions selected from a group consisting of silicon-enriched, wetting layer covered, and a combination thereof.

18. (currently amended) The integrated circuit as claimed in claim 14 wherein the first conformal barrier liner ~~and the second conformal barrier liner are~~comprises a nonconductive barrier materials selected from a group consisting of a nitride, a BLok, a carbide, an oxynitride, and a combination thereof in a thickness between 20 Å and 70Å.

19. (currently amended) The integrated circuit as claimed in claim 14 wherein the first channel dielectric layer~~, the via dielectric layer, and the second channel dielectric layer are of~~comprises a porous low dielectric constant materials having a dielectric constants under 3.9.

20. (currently amended) The integrated circuit as claimed in claim 14 wherein the first conductor core comprises a material ~~and the second conductor core are materials~~ selected from a group consisting of copper, aluminum, gold, silver, compounds thereof, and combinations thereof.